

### Abstract of the Disclosure

A synchronous flash memory includes an array of non-volatile memory cells. The memory array is arranged in rows and columns, and can be further arranged in

5 addressable blocks. Data communication connections are used for bi-directional data communication with an external device(s), such as a processor or other memory controller. A write latch is coupled between the data buffer and the memory array to latch data provided on the data communication connections. The memory can write data to one location, such as a memory array block, while data is read from a second location,

10 such as a second memory array block. The write and read operations are performed on a common addressable row of the array blocks.

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